Appl. No. 10/773,728 Amdt. dated April 26, 2005 Reply to Office Action of February 24, 2005

## **Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

## **Listing of Claims:**

Claim 1 (Currently Amended) A method for processing integrated circuit devices, the method comprising:

providing a monitor wafer, the monitor wafer comprising a silicon material; introducing a plurality of particles within a depth of the silicon material, whereupon the plurality of particles cause the silicon material to be in an amorphous state; introducing a plurality of dopant particles into a selected depth of the silicon

subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant;

material using an implantation tool, the amorphous state trapping the dopant particles;

removing the monitor wafer;

measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer;

determining a dose of the dopant bearing impurities; and operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor water wafer is within a tolerance of a specification limit.

Claim 2 (Original) The method of claim 1 wherein the monitor wafer is substantially free of screen oxide overlying a surface of the monitor wafer.

Claim 3 (Currently amended) The method of claim 1 wherein the plurality of particles are silicon bearing impurities-species.

Claim 4 (Currently Amended) The method of claim 3 wherein the silicon bearing impurities species are implanted using a dose of  $1 \times x = 10^{15}$  atoms/cm<sup>2</sup> and an energy of 20 keV.

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Claim 5 (Original) The method of claim 1 wherein the dopant particles are boron bearing impurities.

Claim 6 (Currently Amended) The method of claim 5 wherein the boron bearing impurities are implanted using a dose ranging from about  $5 \times 10^{13}$   $4 \times 10^{14}$  through  $4 \times 10^{14}$  atoms/cm<sup>2</sup> and an energy ranging from about 1-2 keV.

Claim 7 (Original) The method of claim 1 wherein the thermal anneal process is an RTP process at about 700 Degrees Celsius.

Claim 8 (Original) The method of claim 1 wherein the thermal anneal process is an RTP process ranging from about 650 to 750 Degrees Celsius.

Claim 9 (Original) The method of claim 1 wherein the thermal anneal process is a rapid thermal anneal process.

Claim 10 (Original) The method of claim 1 wherein the sheet resistivity is provided in a separate tool.

Claim 11 (Original) The method of claim 1 wherein the operating of the production wafers occurs for 24 hours after determining the dose of the dopant impurities.

Claim 12 (Original) The method of claim 1 wherein the thermal anneal process also recrystallizes a portion of the amorphous silicon.

Claim 13 (Currently Amended) A method for processing semiconductor waters wafers, the method comprising:

providing a monitor wafer, the monitor wafer comprising a crystalline material; introducing a plurality of particles within a depth of the material, whereupon the plurality of particles cause the crystalline material to be in an amorphous state;

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introducing a plurality of dopant particles into a selected depth of the crystalline material in the amorphous state using an implantation tool, the amorphous state trapping the dopant particles;

subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant;

removing the monitor wafer;

measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer;

determining a dose of the dopant bearing impurities; and

operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor water is within a tolerance of a specification limit.

Claim 13 14 (Currently Amended) The method of claim 12 13 wherein the crystalline material comprises silicon.

Claim 14 15(Currently Amended) The method of claim 12 13 wherein the dose of the dopant bearing impurities is determined using a relationship between resistivity values and dose values.

Claim 45 16 (Currently Amended) The method of claim 44 15 wherein the relationship has been provided in a spatial plot.

Claim 16 17 (Currently Amended) The method of claim 12 13 wherein the plurality of particles comprise silicon bearing particles.

Claim 47 18 (Currently Amended) The method of claim 42 13 wherein the dopant bearing impurities comprise boron species.

Claim 18 19 (Currently Amended) The method of claim 11 13 wherein the monitor water is substantially free from an overlying oxide layer before introducing the dopant bearing impurities.

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Claim  $\frac{19}{20}$  (Currently Amended) The method of claim  $\frac{11}{12}$  wherein the monitor wafer is  $\underline{a}$  silicon wafer.

Claim 20 21 (Currently Amended) The method of claim 11 13 wherein the one or more production wafers is characterized by a shallow junction depth of less than about 40 nm.